

VLSI Design

Lecture 11: Managing the Delay of Combinational Networks

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Adapted from lecture notes prepared by the author (from
Prentice Hall PTR)

Topics

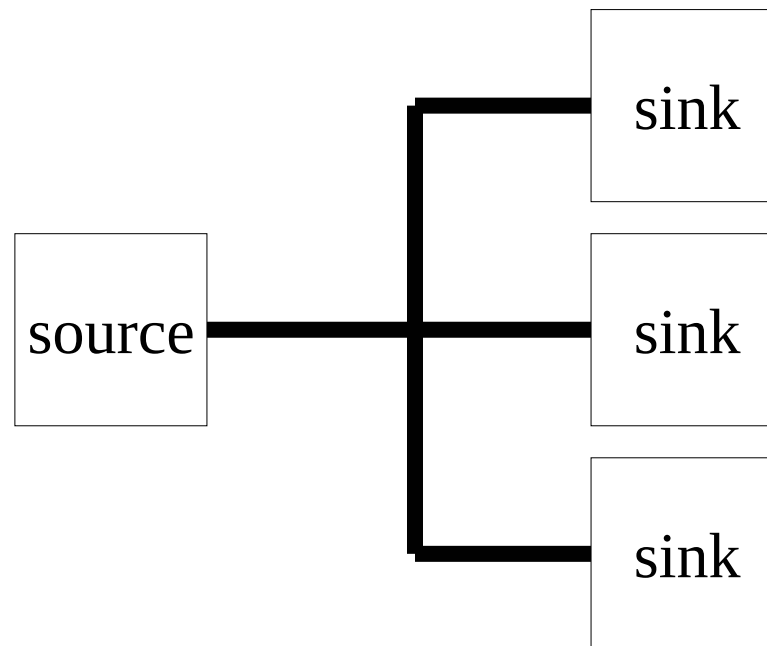
- Combinational network delay
- Path delay
- Logic optimization

Sources of delay

- Gate delay:
 - drive;
 - load.
- Wire:
 - lumped load;
 - transmission line.

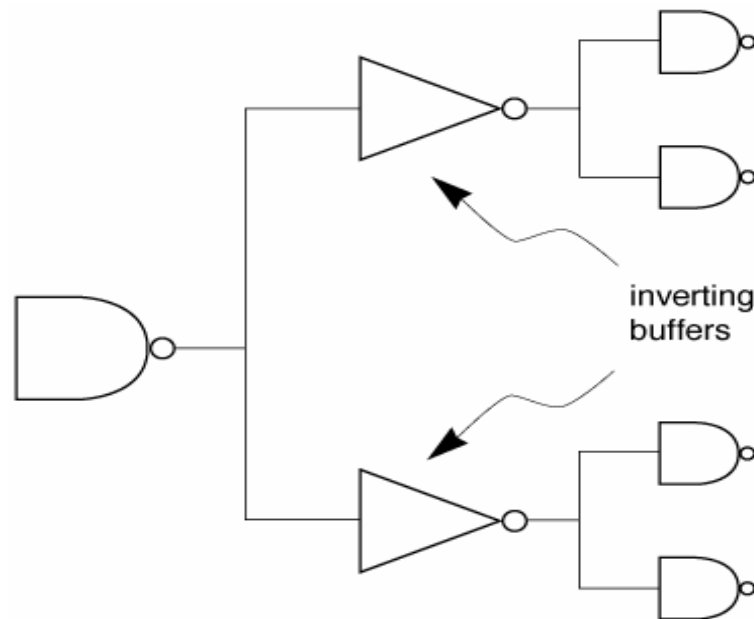
Fanout

- Fanout adds capacitance.



Ways to drive large fanout

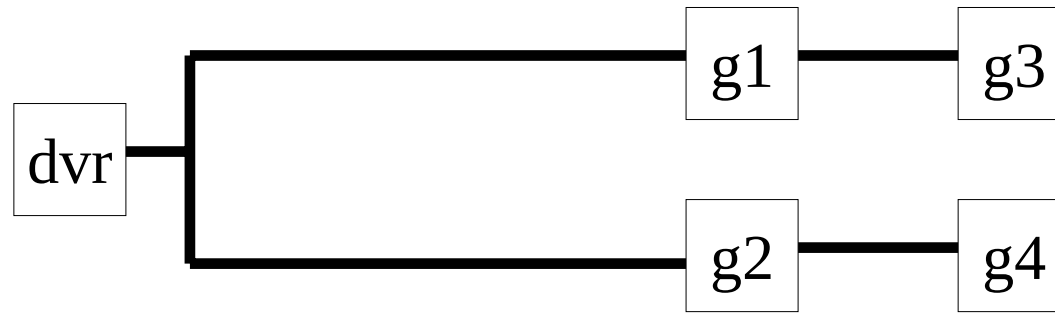
- Increase sizes of driver transistors. Must take into account rules for driving large loads.
- Add intermediate buffers. This may require/allow restructuring of the logic.



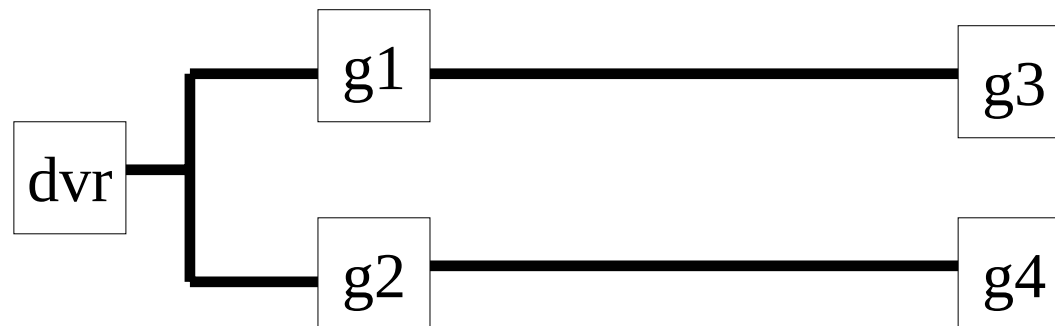
Wire capacitance

- Use layers with lower capacitance.
- Redesign layout to reduce length of wires with excessive delay.

Placement and wire capacitance



unbalanced load



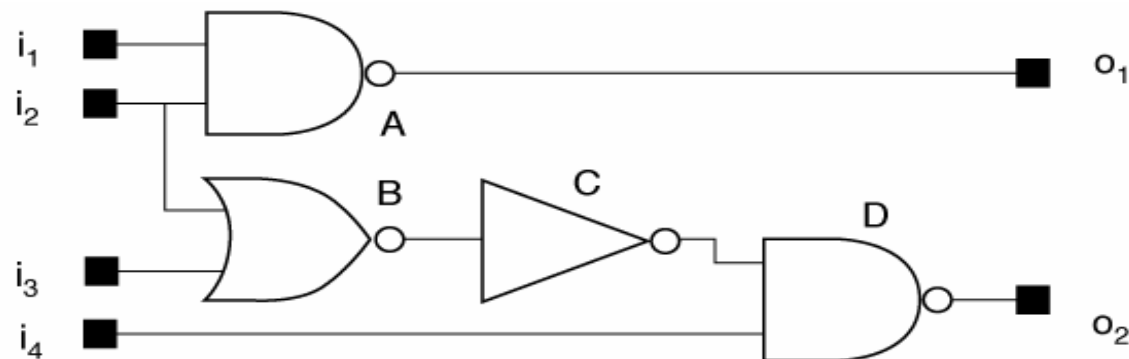
more balanced

Path delay

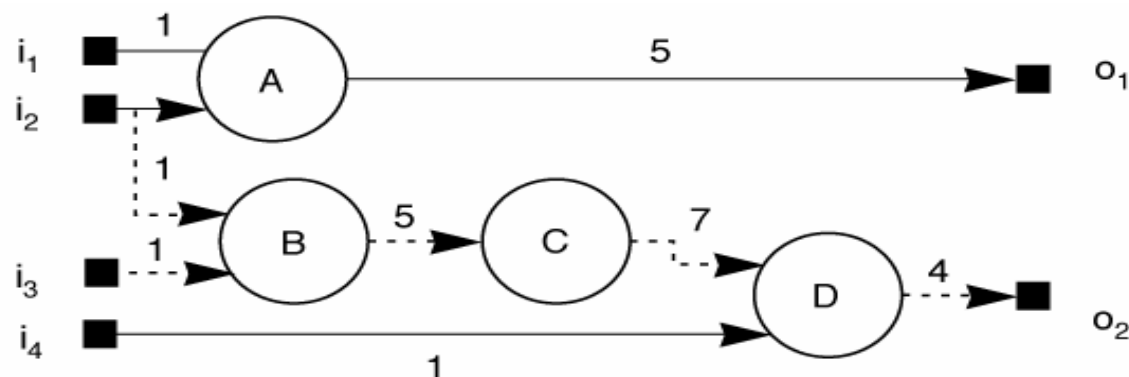
- Combinational network delay is measured over paths through network.
- Can trace a causality chain from inputs to worst-case output.
- Critical path = path which creates longest delay.
- Can trace transistions which cause delays that are elements of the critical delay path.

Delay model

- Nodes represent gates.
- Assign delays to edges; signal may have different delay to different sinks.
- Lump gate and wire delay into a single value.

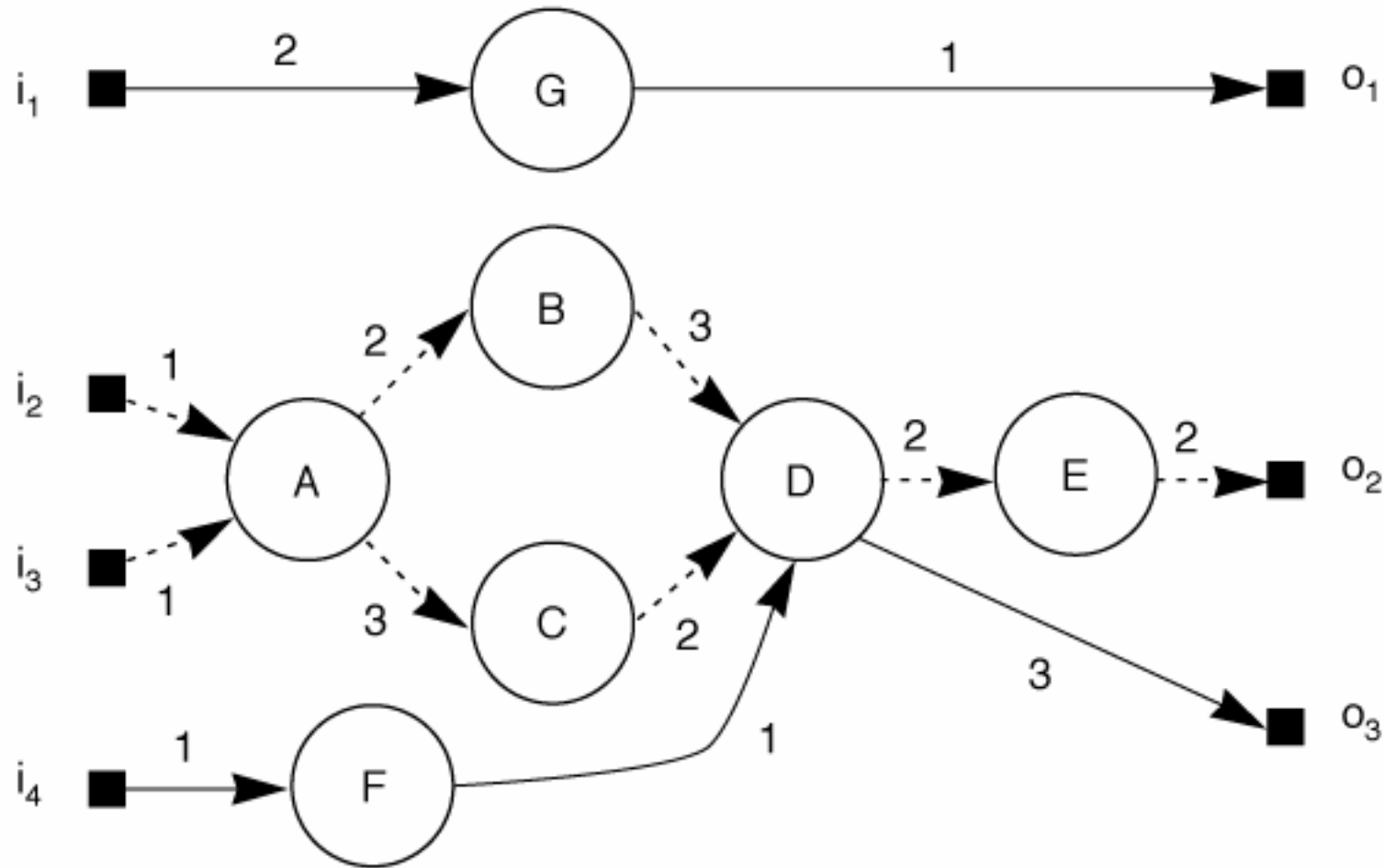


network



graph model

Critical path through delay graph

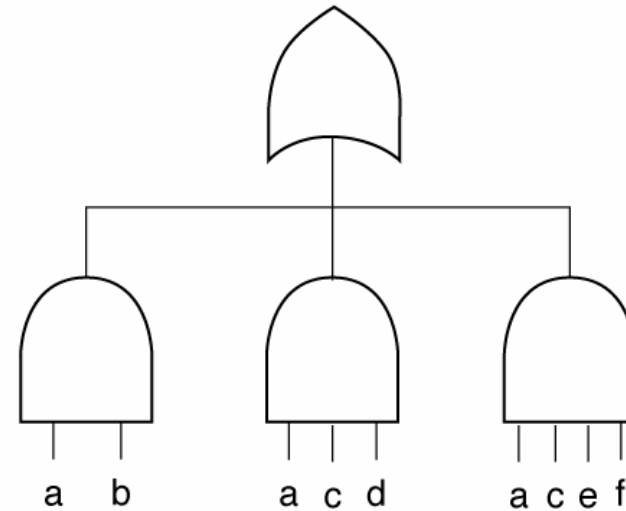
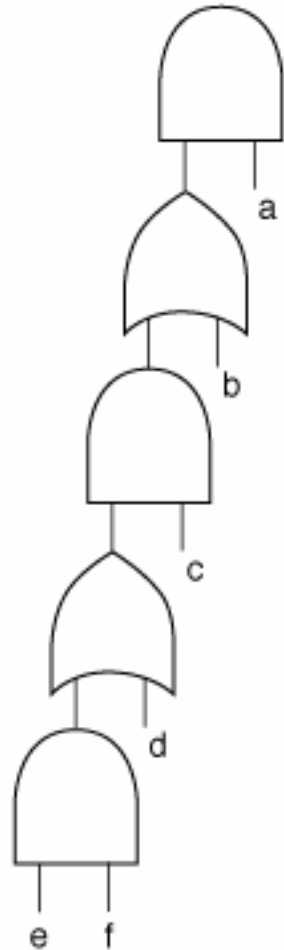


Reducing critical path length

- To reduce circuit delay, must speed up the critical path.
 - reducing delay off the path doesn't help.
- There may be more than one path of the same delay. Must speed up all equivalent paths to speed up circuit.
- Must speed up cutset through critical path.

Logic rewrites

deep logic



shallow
logic

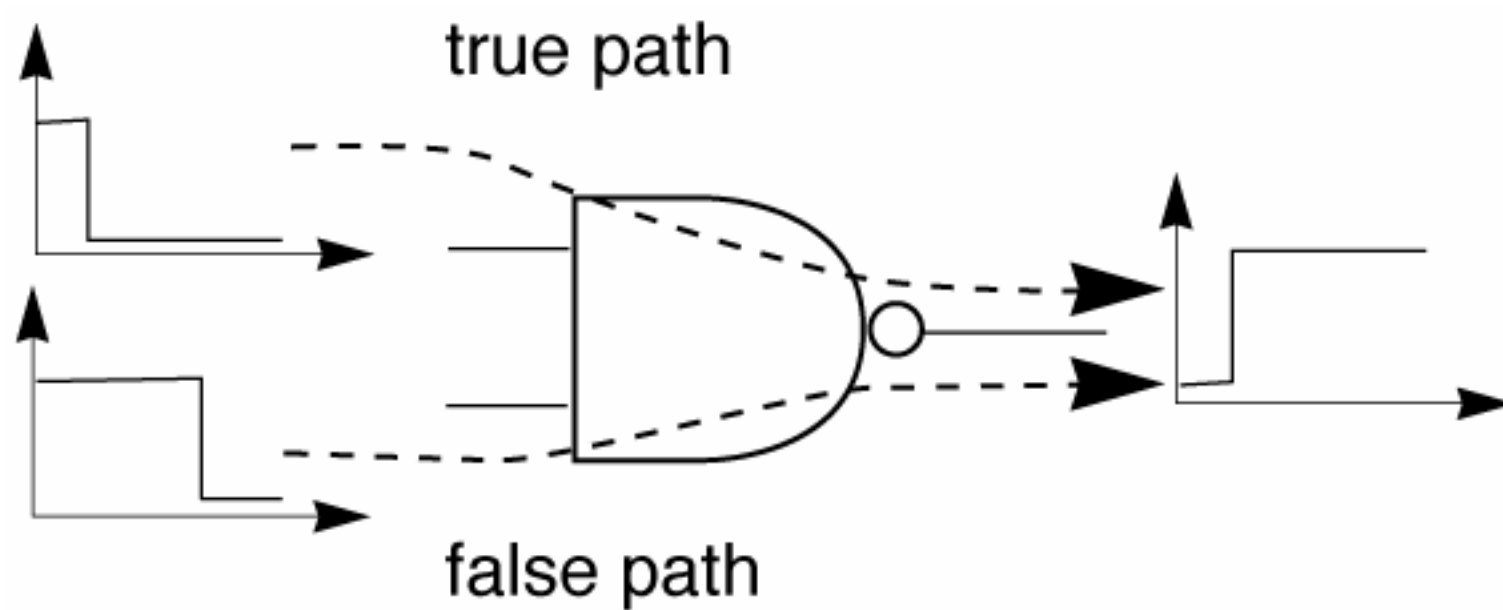
Logic transformations

- Can rewrite by using sub-expressions.
- Flattening logic increases gate fanin.
- Logic rewrites may affect gate placement.

False paths

- Logic gates are not simple nodes; some input changes don't cause output changes.
- A false path is a path which cannot be exercised due to Boolean gate conditions.
- False paths cause pessimistic delay estimates.

False path example



Logic optimization

- Logic synthesis programs transform Boolean expressions into logic gate networks in a particular library.
- Optimization goals: minimize area, meet delay constraint.

Technology-independent optimizations

- Works on Boolean expression equivalent.
- Estimates size based on number of literals.
- Uses factorization, resubstitution, minimization, etc. to optimize logic.
- Technology-independent phase uses simple delay models.

Technology-dependent optimizations

- Maps Boolean expressions into a particular cell library.
- Mapping may take into account area, delay.
- May perform some optimizations in addition to simple mapping.
- Allows more accurate delay models.